

Solving Electromagnetic Coupling Problems by Spatial Component Placement.

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ABSTRACT

More and more demand is being placed on The Appliance Industry to meet Global Electromagnetic Compatibility performance standards. The sophistication of these appliances with the use of electronic controls and switching power supplies increases the challenge of solving EMC problems. The most effective way of solving EMC problems is to intervene at the interference sources, i.e. to tackle them at the component placement level. Several EMC phenomena take place in electronic circuits, which can be minimized by using simple placement rules.

In this article, guidance is given on component placement considerations that affect the performance of shielding and filtering. These are in the form of proximity rules that govern spacing between noisy integrated circuit devices and ventilation screens, internal connectors and filter devices. Special attention is given to Filter component placements (spatial orientation) to minimize magnetic coupling.

INTRODUCTION

The sophistication of today's home appliances with the use of electronic controls and switching power supplies increases the challenge of solving EMC problems. It is a known fact that the most effective way of solving EMC problems is to intervene at the sources, on the printed circuit board (PCB).

Many CAD software and design processes include Layout and component placement rules to help achieve signal integrity and EMC.

The Design review process is divided into 3 phases, which are considered crucial in the development of an electronic circuit.

They are;

- Schematic review,
- Component Placement review
- Layout review.

Costly, Electromagnetic problems can be avoided by using guidelines outlined in this article.

SCHEMATIC REVIEW

Clock

Select the slowest clock rate and the slowest technology that the circuit function allows. This will also minimize the cost. If high clock speeds are essential, give preference to clock higher clock rate internal to the IC, which is locked to a lower external clock rate. It is preferable that the higher clock rate remains internal to the IC to contain most of the emission power. Clock frequencies should be selected to minimize or eliminate harmonic overlap. By keeping harmonics > 120 kHz apart, overlap "aliasing" should be eliminated. Slew resistors may be used on clocks to suppress rise times, which in turn will lower higher frequency clock harmonics.^{[1][2][3][7]}

In order to prevent ringing, overshoot and undershoot, clock and signal traces

should be properly terminate. Unpopulated traces should be terminated to ground to allow a return path for surface current.^{[1][3][7]}

Signal Lines

All input and output power and signal lines that connect to system cables should be filtered with: common mode chokes, differential mode inductors, or capacitors.^{[1][3][7]}

There must be, at the very least, an LC filter at the power feed in order to aid in reducing conducted emissions. These filters should be placed as near as possible to the power entry. Power supplies or power converters will probably require common-mode and differential-mode filtering. They are noisy devices, which can cause both conducted and radiated problems.

Capacitors

Capacitors are used for various functions within a PCB, including minimizing ground bounce, shunting RF energy, and removing common-mode and differential-mode RF currents.^{[1][3][7]}

Capacitors are used in one of three configurations:

- decoupling,
- bypassing,
- bulk.

Decoupling is provided at the component level to prevent ground-noise voltage and high frequency voltage spikes from being injected into the power and ground plane structure.^{[1][3][7]}

The Attenuation curve in Figure 1 present results of decoupling capacitor between a ground plane and a power plane.

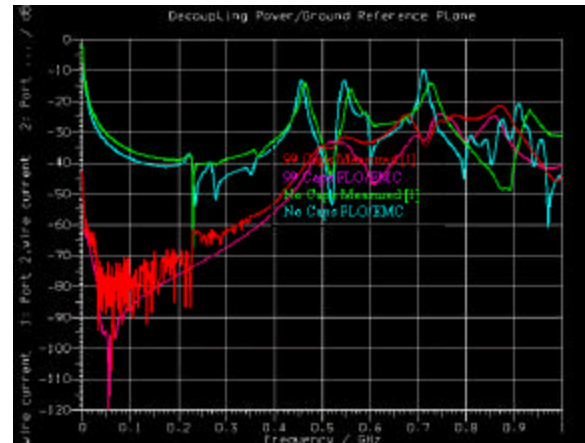


Figure 1. Ground plane radiation with/without decoupling capacitors.^[5]

Bypass capacitors divert differential mode currents from signal cables, thus allowing only the desired data to be present. They do this by removing the alternating currents usually caused by ripple voltage.^{[9][1]}

Bulk capacitors keep the unit functioning by insuring that sufficient voltage is present for all circuits under maximum power consumption usage. They also help prevent ground bounce from occurring.^{[1][3][9]}

Surface mount decoupling capacitors provide the best attenuation. However, trace lengths between the components and the power connections should be kept to a minimum. Decoupling capacitors need to have low loss and high resonant frequencies in order to be efficient. Multiple decoupling capacitors can lead to self-resonance. To prevent self-resonance, each capacitor should be different by at least two orders of magnitude.

ICs and Logic Families

All unused ports on devices and on modules should be terminated.

Surface mount components provide the best EMI characteristics. If a heat sink is used it should be isolated from the ICs by thermal conductor and should be RF bonded at multiple points to the ground plane. If no ground points are available it may be better in some instances, to leave the heat sink floating.^{[1][3]}

Figure 2 below show a simulation of a heat sink emission patterns. The EMI from this can be suppress with good grounding.

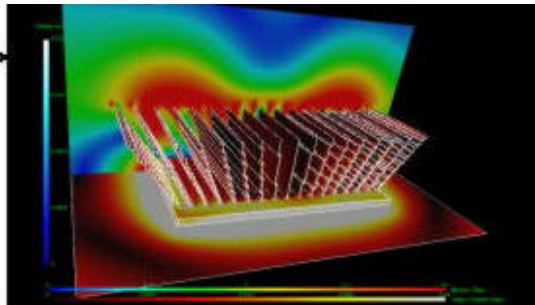


Figure 2. Floating Heat sink radiation pattern.^[5]

Integrated circuits should be chosen for its advanced signal integrity and EMC features:

IC should feature:

- Adjacent power and ground pins;
- Multiple power and ground pins;
- Suppressed output voltage swing;
- Controlled slew rates;
- Transmission-line matching signals;
- Differential signalling;
- Low ground bounce;

- Low levels of emissions;
- High levels of immunity to ESD and other disturbing phenomena;
- Low input capacitance;
- Output drive capability no larger than needed for the application;
- Low levels of power supply transient currents (sometimes called "shoot-through currents").

Connectors and Interconnect

Use partitioning in the connector section. Separating reset lines from clock lines and noisy signals from quiet signals can significantly suppress noise emissions. Lower speed signals should be placed on connector pins that have longer paths. Ground pins should surround all single ended 50 Mbps or higher frequency signals. Place at least one ground pin beside each noisy signal and ground pin should be placed next to sensitive lines like reset lines.

Use more than one connector pin for power input and return, if necessary, to suppress the voltage drop across the contacts. Any electrical connections with external cabling must be properly filtered on the PCB. The purpose of the filter is to remove any unnecessary high frequency components from the transmitted signal, which could potentially cause severe, radiated and conducted emissions on the cable. Any cable exiting a shielded enclosure is a potential EMI radiator.

GUIDELINES FOR COMPONENT PLACEMENT

General

A critical signal floor plan should be developed. Clock and high-speed

data signals should be identified. Trace carrying signals from the source to the destination should be as short as possible. Components must be placed to minimize track length of critical signals.

Storage capacitors should be placed as close to the location where demand is the greatest. ^{[1][3]}

Filtering for electrical connections with external cabling should be placed at the point of entry on the PCB. If common mode chokes are employed, ground planes should not be present underneath the chokes. This is to help reduce magnetic coupling. Decoupling can be improved by placing Coil and transformer horizontally instead of vertically in some circuit layout. ^[1]

Clock generation components should be located near the signal section or centre of the PCB rather than along the perimeter of the board. Using different areas for low, medium, and high-speed logic can help suppress aliasing and cross talk. ^[3]

Component Proximity Effects

High-speed devices shall be located a minimum of 25 mm. from all connectors, to suppress direct coupling between the device and the connector pins. High frequency components, such as clocks or ICs, should not be placed close to any openings or interfaces where they may radiate easily through nearby holes. High frequency components, as well, should generally be placed at least 25 mm from power converters and power filters. This should prevent high frequency noise from escaping onto ground or power traces.

All components, except those that interface with the outside world, should not be placed in areas where they will be susceptible to ESD discharges. Components such as high-speed integrated circuits produce relatively strong magnetic and electric fields in their immediate vicinity at the frequencies ranging from the fundamental to frequencies over 1 GHz.

Shielding effectiveness of a ventilation screen or aperture varies with proximity of a magnetic field source such as an IC. As a general rule, a 25 mm. or greater spacing between IC's and ventilation screens and other apertures should be maintained.

Keep threat traces and the devices that produce them away from the edges of the PCB to minimize coupling to objects near the PCB and to maintain a low return impedance. This should also help with ESD discharges. Position all threat traces and the devices that generate them away from signal devices and connectors. Table 1 and Figure 3 gives some proximity rules for IC placement. ^{[6][3]}

Table 1. Proximity Rules to Minimize Printed Circuit Board EMI Coupling. [3]

Description	Figure 3	Proximity	Comments
IC Close to Vent Panel	A	>25 mm	To suppress IC coupling through vent
IC Close to PCB Edge	B	>15 mm	To suppress PCB Edge currents
PCB Edge to Vent Panel	C	>5 mm	To suppress edge coupling to vent
IC Close to signal Connector	D	>35 mm	To suppress noise load on signal filters
IC Close to PCB Edge Connectors	E	>25 mm	For signal circuits
IC Close to POWER SUPPLIES OR POWER CONVERTER EMI Filter	F	>35 mm	Important if POWER SUPPLIES OR POWER CONVERTER filter unshielded
IC Close to Aperture	G	>25 mm	Depends on aperture size
Surface Clock Trace to Vent	H	>25 mm	To suppress coupling through vent
Surface Clock Trace to PCB Edge	I	>15 mm	To suppress PCB edge currents
Surface Clock Trace to signal Connector	J	>35 mm	To suppress noise load on signal filters

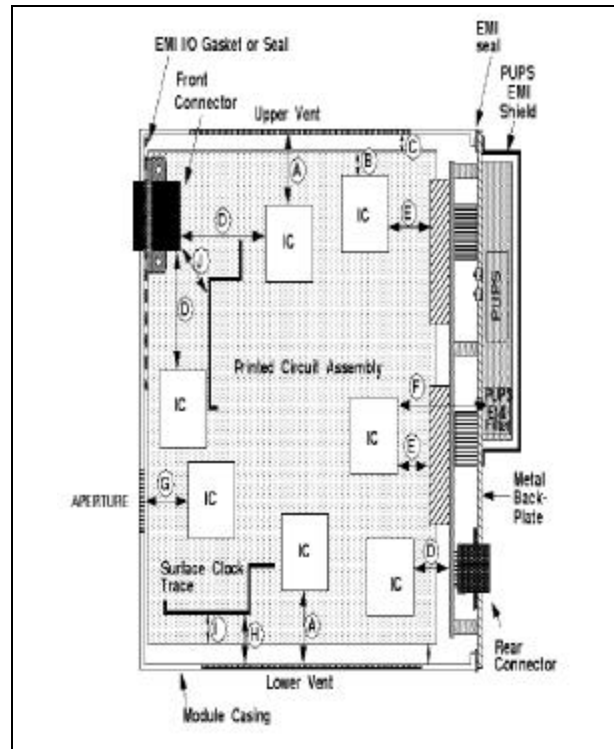


Figure 3. Proximity Rules to Minimize Coupling on Printed Circuit Board [3]

To optimize component placement, numerical simulation software can be used. Such tools can be used to visualize field effect in an enclosure. This can help the designer to avoid hot spots. Figure 4 below show the EM field distribution over a populated circuit board.

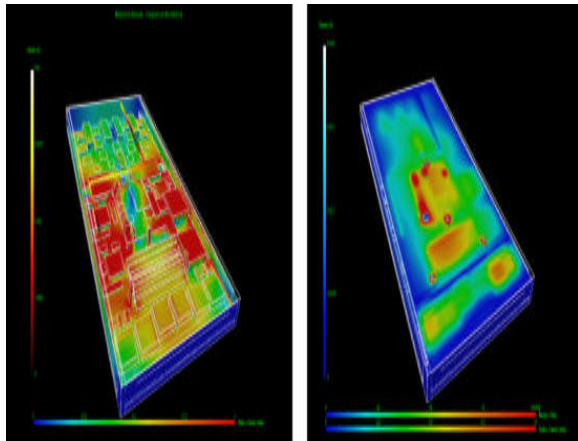


Figure 4. E-Field Distribution on a populated PCB. [5]

Guidelines for PCB Layout

Multi-Layer boards

Selection of layer stack up is always very dependent on the detailed application. The following rules should be applied to multi-layer boards;

- Use embedded capacitance or buried capacitance technology if available.
- Use adjacent power and 0V planes to maximize capacitance and suppress emissions.
- Use a thin dielectric between adjacent power and 0V planes to improve their decoupling performance.

Clocks, Periodic and High Speed Signals

Clock and periodic signal traces should always be *manually* routed first.

Route all clock lines with 25 - 50 mil separation from other signals. It is important to keep clock traces far from the edges of the board to eliminate EM jumping and coupling. When a jump is made from a horizontal to a vertical routing layer, the RF return current *cannot* make this jump due to the discontinuity occurring at the trace route from the via. The RF return current must find an alternate low impedance path to ground. A suitable alternate path usually does not exist when jumping a trace between layers.

To minimize creation of EMI and cross talk, due to layer jumping, the following design techniques have been found to be effective: [1][3][7][9]

- Route all clock and high-threat signal traces on only one routing layer. This means that both “x” and “y” axis routes are on the same plane.
- Verify that a solid 0V reference, or ground plane, is adjacent to the routing layer with no discontinuities in the route, e.g., plane cuts or moats.
- If a via must be used for routing a sensitive, high-threat, or clock signal trace between horizontal and vertical routing layers, incorporate corresponding ground vias at each and

every via location where the axis jump occurs.

Inductance in a trace can cause both signal integrity concerns (time domain) and potential RF emissions (frequency domain). If a periodic signal, or clock trace, must traverse from one routing plane to another, this transition should occur only at the component lead ground reference. The reason for making the transition adjacent to a component lead is to allow RF return current to easily make a layer transition jump. Try for a maximum of two vias per route, one at the source, and one at the load, if a strip line configuration is provided. ^{[1][3][7][9]}

Rules to Minimize Cross talk:

Threat traces can couple capacitive or inductively to nearby traces. A certain minimum spacing is required between traces to keep cross talk to a minimum. Here are some general rules of thumb:^{[7][9][10]}

- Separate parallel traces by 0.05 mm. for every inch of common trace length.
- Separate threat traces from others by a spacing equal to 3 times the centre-to-centre distance between the trace and its return.
- Ensure physical spacing between traces. For clock traces the trace edge-to-edge separation distance, S, shall be a minimum of 3 times the trace height, H, hence $S/H \geq 3$. For data traces, $S/H \geq 1$.
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Power and Ground

Planes must not be floating or isolated on a Circuit board. For high-speed boards, use embedded capacitance technology which sandwiches power and ground planes in very close proximity. If embedded capacitance technology is not available, place power and ground planes adjacent to each other in the stack up to maximize capacitive coupling and suppress power supply noise. For high-speed boards, use extra ground planes and connect them with vias to allow return ground paths to follow signals as closely as possible. Ground plane should be kept away from common mode chokes.

Differential Signals

All differential pairs must travel as close as possible to each other in order to reduce the loop area, and thus the emissions. All single-ended signals should be routed as directly as possible in such a way that their total length is kept to a minimum. If differential noise is problematic and differential coils are used, these coils should be parallel to each other with a minimum distance between the two windings. Coils should also be kept far from Transformer or power inductors to eliminate magnetic coupling. ^{[1][3][5][7]}

Reset & Interrupt Signals

Reset and interrupt lines should have more than 50-mil space from other noisy signal tracks. Damping resistors may be required for long reset/interrupt tracks to suppress any line effect. ^{[7][3]}

CONCLUSION

There are numerous rules to follow for a good PCB review. These rules can help increase the integrity of the product. However only the EMC test can confirm the compliance. By applying the above rules most EMC problem should be eliminated or reduced.

The Appliance industry tends to use single layer boards due to cost. However, with the increase use of microprocessors, the Appliance industry may find it more economical to use multi-layer boards since it can reduce costly shielding and filtering.

- [1] Isidor Straus, entitled "18 Rules to Follow for Better Digital EMC Design," *Conformity* magazine, Vol. 3, No. 1, January 1998, ISSN 1094-2459.
- [2] Patrick Mannion, "Minimize The Effects Of EMI And Let Your Design Do Its Job", *ELECTRONIC DESIGN* - April 19 1999 Volume.
- [3] Mark I. Montrose, "EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple", Series Affiliation : IEEE Press Series on Electronics Technology. ISBN 0-7803-4703-X.
- [5] <http://www.flomerics.com>
- [6] Warren Boxleitner, *Electrostatic discharge and electronic equipment*, IEEE Press, 1989

- [7] Howard W. Johnson and Martin Graham, "*High-speed digital design*", PTR Prentice Hall, 1993.
- [8] MIL-HDBK-241B, 1983: Design Guide for Electromagnetic Interference (EMI) Reduction in Power Supplies
- [9] Henry W. Ott, "*Noise reduction techniques in electronic systems*", John Wiley & Sons, 1988